Shinnung Jeong

Curriculum Vitae

Contact Information

School of Electrical and Electronic Engineering
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Education

Yonsei University, Seoul, Republic of Korea
Integrate M.S./Ph.D. Student, March 2019 to Present
Advisor: Prof. Hanjun Kim

Pohang University of Science and Technology (POSTECH), Pohang, Republic of Korea
Bachelor of Science in Creative IT Engineering, March 2015 to February 2019

Gwangju Science Academy for the Gifted, Gwangju, Republic of Korea
High school, March 2013 to February 2015

Experience

Research Assistant, March 2019 to Present
Compiler Research Laboratory (Corelab), *Younsei University*, Seoul, Republic of Korea

- Develop thread-aware area optimized high-level synthesis framework for IoT devices (CGO 2021)
- Design dynamic neural networks for real-time systems (ECRTS 2022)
- Design graph processing interface to enlarge design space for GPU (PACT 2022)
- Develop locality-aware graph topology layout for GPU

Visiting Scholar, March 2023 to Present
High Performance Architecture Lab(HPArch), *Georgia Institute of Technology*, Atlanta, Georgia, USA

- Advisor : Prof. Hyesoon Kim
- Develop compiler of the Open Source GPU, Vortex GPU.
- Expand the application support of the Vortex GPU.

Undergraduate Research Assistant, December 2017 to June 2018
Compiler Research Laboratory (Corelab), *POSTECH*, Pohang, Republic of Korea

- Develop interactive outdoor advertisement system that recommends advertisements based on eyes pose, facial expression, age, and gender data

Undergraduate Research Assistant, June to August 2016, January to February 2017
POSTECH Database and Data Mining Lab (Big data lab), *POSTECH*, Pohang, Republic of Korea

- Design Natural Language processing system for Korean

Undergraduate Student Intern, September to December 2016
Excem, Pohang, Republic of Korea

- Develop alarm system and web UI for cloud server

Exchange Student, September to December 2015
University of California, Berkeley, United States of America

Recognition

- Magna Cum Laude from POSTECH, February 2019
- Excellence Award, Creative IT Design Competition, Department of Creative IT Engineering, POSTECH, June 2018
- PJ Metal Best Papers, Department of Humanities and social sciences, POSTECH, December 2018
- Excellence Award, 2018 POSTECH Hackathon Catch, PoApper, November 2018
- Excellence Award, Arthackathon : Next-generation culture and arts education with 4th Industrial Revolution Technology, Jun 2018
- The Grand Prize, Create IT Design Competition, Department of Creative IT Engineering, POSTECH, June 2016
- Vadas Award, Create IT Design Competition, Department of Creative IT Engineering, POSTECH, December 2016 (Award given to the most commercially successful project)
- Vadas Award, Create IT Design Competition, Department of Creative IT Engineering, POSTECH, June 2016

Activities

International Conference Reviewer

- Reviewer, Transactions on Architecture and Code Optimization (TACO), 2023

International Conference Sub-reviewer

- Sub-reviewer, The ACM/IEEE International Symposium on Code Generation and Optimization (CGO), 2022, 2021, 2020
- Sub-reviewer, IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2022, 2021
- Sub-reviewer, The 25th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2020
- Sub-reviewer, 2019 IEEE Micro, 2019

Teaching

- EEE3313-01: Basic Digital Experiments, Yonsei University
  Teaching Assistant, Spring 2021
  Teaching Assistant, Fall 2020
  Teaching Assistant, Spring 2019
  (Teaching weekly lab classes about how to writing RTL Verilog code and designing hardware acceleration(FPGA-ARM))
- EEE3540-01: Microprocessor, Yonsei University
  Teaching Assistant, Fall 2019
  (Teaching weekly lab classes about programming related to microprocessor)

Publications

Refereed Journal Publications

[1] Bongjun Kim, Seonyeong Heo, Jaeho Lee, Shinnung Jeong, Yongwoo Lee, and Hanjun Kim, "Compiler-assisted Semantic-aware Encryption for Efficient and Secure Serverless Computing," in *IEEE Internet of Things Journal*, April 2021.
IF=9.936, Q1 (JCR 2019)

Refereed Conference Publications

[2] Jaeho Lee, Shinnung Jeong, Seungbin Song, Kunwoo Kim, Heelim Choi, Youngsok Kim, and Hanjun Kim, "Occamy: Memory-efficient GPU Compiler for DNN Inference," in *Proceedings of the 60th Annual Design Automation Conference 2023 (DAC)*, July 2023.

[3] Shinnung Jeong, Yongwoo Lee, Jaeho Lee, Heelim Choi, Seungbin Song, Jinho Lee, Youngsok Kim, and Hanjun Kim, "Decoupling Schedule, Topology Layout, and Algorithm to Easily Enlarge the Tuning Space of GPU Graph Processing," in *31st International Conference on Parallel Architectures and Compilation Techniques (PACT)*, October 2022.

[4] Seonyeong Heo, Shinnung Jeong, and Hanjun Kim, "RTScale: Sensitivity-Aware Adaptive Image Scaling for Real-Time Object Detection," in *34th Euromicro Conference on Real-Time Systems (ECRTS)*, July 2022.

[5] Yongwoo Lee, Seonyeong Heo, Seonyoung Cheon, Shinnung Jeong, Changsu Kim, Eunkyung Kim, Dongyoon Lee, and Hanjun Kim, "HECATE: Performance-Aware Scale Optimization for Homomorphic Encryption Compiler," in *Proceedings of the 2022 International Symposium on Code Generation and Optimization (CGO)*, April 2022.

[6] Changsu Kim, Shinnung Jeong, Sungjun Cho, Yongwoo Lee, William Song, Youngsok Kim, and Hanjun Kim, "Thread-Aware Area-Efficient High-Level Synthesis Compiler for Embedded Devices," in *Proceedings of the 2021 International Symposium on Code Generation and Optimization (CGO)*, March 2021.

Refereed Poster Publications

[7] Changsu Kim, Yongwoo Lee, Shinnung Jeong, and Hanjun Kim, "Logic Deduplication with Decentralized Pointer Analysis in HLS for Post-Quantum Cryptography Algorithms," in *Proceedings of the 57th Annual Design Automation Conference 2020 - (Poster) (DAC)*, July 2020.

[8] Changsu Kim, Yongwoo Lee, Shinnung Jeong, Wen Wang, Jakub Szefer, and Hanjun Kim, "Pipeline-aware Logic Deduplication in High-Level Synthesis for Post-Quantum Cryptography Algorithms," in *Proceedings of the 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, February 2020.